WHERE TO START WITH YOUR 6023E/6024E/6025E

Thank you for buying a National Instruments 6023E, 6024E, or 6025E board. The 6025E features 16 channels (eight differential) of analog input, two channels of analog output, a 100-pin connector, and 32 lines of digital I/O. The 6024E features 16 channels of analog input, two channels of analog output, a 68-pin connector and eight lines of digital I/O. The 6023E is identical to the 6024E, except that it does not have analog output channels. The 6023E, 6024E, and 6025E kits include NI-DAQ driver software, which provides an extensive library of functions for digital I/O boards and other devices.

Documentation

6023E/6024E/6025E

For detailed information about the 6023E, 6024E, or 6025E, see the *6023E/6024E/6025E User Manual.* This manual is available in electronic format on your NI-DAQ software distribution CD. If you prefer a hard copy of this manual, you can print it from the Acrobat reader or you can order a printed, bound copy from National Instruments (part number 322072B-01).

The user manual provides signal connection information, a hardware overview, and product specifications. The manual also contains warranty information and important warnings explaining the correct use of the 6023E, 6024E, and 6025E.

NI-DAQ

If you are using NI-DAQ as your software interface to the 6023E, 6024E, or 6025E, install the NI-DAQ software documentation from the NI-DAQ distribution CD in addition to installing the 6023E/6024E/6025E hardware documentation.

If you are using software other than NI-DAQ, use the documentation included with that software.

322153B-01 *December 1998*

Installation

Software and Documentation

If you are using software other than NI-DAQ, consult your software documentation for software installation instructions.

Refer to the NI-DAQ release notes to install the NI-DAQ software and related documentation. When prompted during the software installation process to select components, select the option to install documentation. Choose the *6023E/6024E/6025E User Manual* and any other documents you want, such as the NI-DAQ software documents.

To install the hardware documentation without installing NI-DAQ software, deselect all components other than the documentation option.

Hardware

☞ **Note** ***Install your software before you install your board.***

After installing your software, you are ready to install your hardware. Your board will fit in any 5 V expansion slot in your computer. However, to achieve best noise performance, leave as much room as possible between your board and other devices. The following are general installation instructions. Consult your computer user manual or technical reference manual for specific instructions and warnings.

- PCI Board Installation
  1. Write down your board's serial number in the 6023E/6024E/6025E Hardware and Software Configuration Form in Appendix D, *Customer Communication*, of the *6023E/6024E/6025E User Manual*.
  2. Turn off and unplug your computer.
  3. Remove the top cover of your computer.
  4. Remove the expansion slot cover on the back panel of the computer.
  5. Insert the board into a 5 V PCI slot. Gently rock the board to ease it into place. It may be a tight fit, but *do not force* the board into place.
  6. Screw the mounting bracket of the board to the back panel rail of the computer.
  7. Replace the top cover of your computer.
  8. Plug in and turn on your computer.

- PXI Board Installation

  1. Write down your board's serial number in the 6023E/6024E/6025E Hardware and Software Configuration Form in Appendix D, *Customer Communication,* of the *6023E/6024E/6025E User Manual*.
  2. Turn off and unplug your computer.
  3. Choose an unused PXI slot in your system. For maximum performance, the PXI E Series board has an onboard DMA controller that can only be used if the board is installed in a slot that supports bus arbitration, or bus master cards. National Instruments recommends installing the PXI E Series board in such a slot. The PXI specification requires all slots to support bus master cards, but the CompactPCI specification does not. If you install in a CompactPCI non-master slot, you must disable the PXI E Series board onboard DMA controller using software.
  4. Remove the filler panel for the slot you have chosen.
  5. Insert the PXI E Series board into a 5 V PXI slot. Use the injector/ejector handle to fully insert the board into the chassis.
  6. Screw the front panel of the PXI E Series board to the front panel mounting rail of the system.
  7. Plug in and turn on your computer.

  The board is installed. You are now ready to configure your software. Refer to your software documentation for configuration instructions.

I/O Connector

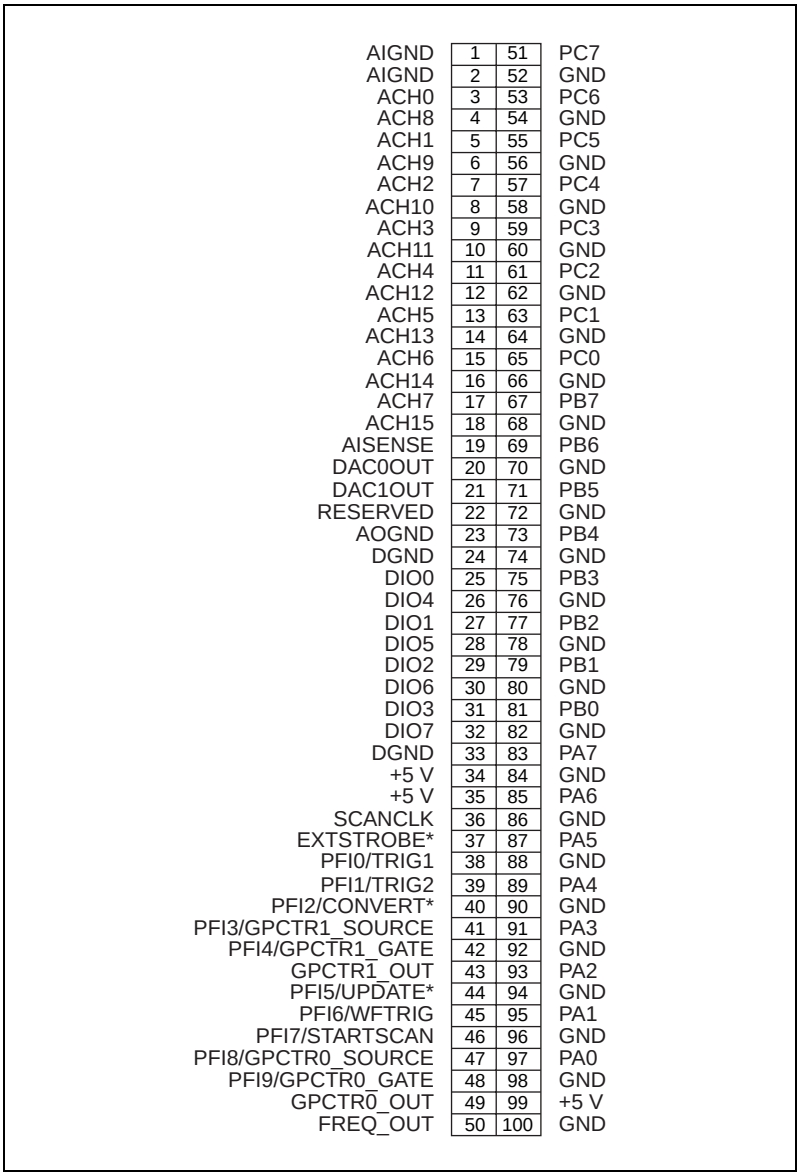
Figure 1 shows the pin assignments for the 68-pin I/O connector on the 6023E and 6024E. It is also the MIO-16 68-pin connector available when you use the SH1006868 cable assembly with the 6025E.

ACH8	34	68	ACH0
ACH1	33	67	AIGND
AIGND	32	66	ACH9
ACH10	31	65	ACH2
ACH3	30	64	AIGND
AIGND	29	63	ACH11
ACH4	28	62	AISENSE
AIGND	27	61	ACH12
ACH13	26	60	ACH5
ACH6	25	59	AIGND
AIGND	24	58	ACH14
ACH15	23	57	ACH7
DAC0OUT[1]	22	56	AIGND
DAC1OUT[1]	21	55	AOGND
RESERVED	20	54	AOGND
DIO4	19	53	DGND
DGND	18	52	DIO0
DIO1	17	51	DIO5
DIO6	16	50	DGND
DGND	15	49	DIO2
+5 V	14	48	DIO7
DGND	13	47	DIO3
DGND	12	46	SCANCLK
PFI0/TRIG1	11	45	EXTSTROBE*
PFI1/TRIG2	10	44	DGND
DGND	9	43	PFI2/CONVERT*
+5 V	8	42	PFI3/GPCTR1_SOURCE
DGND	7	41	PFI4/GPCTR1_GATE
PFI5/UPDATE*	6	40	GPCTR1_OUT
PFI6/WFTRIG	5	39	DGND
DGND	4	38	PFI7/STARTSCAN
PFI9/GPCTR0_GATE	3	37	PFI8/GPCTR0_SOURCE
GPCTR0_OUT	2	36	DGND
FREQ_OUT	1	35	DGND

[1] Not available on the 6023E

Figure 1. I/O Connector Pin Assignment for the 6023E and 6024E

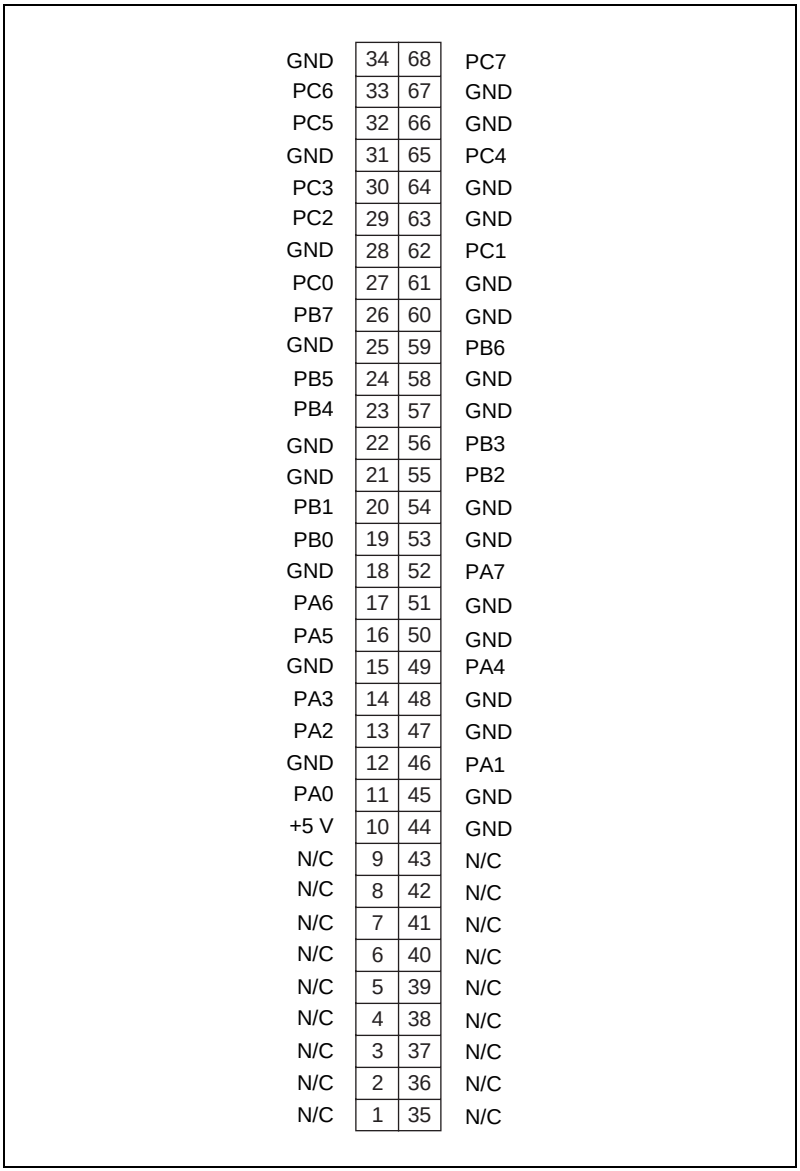
Figure 2 shows the pin assignments for the 100-pin I/O connector on the 6025E.



AIGND	1	51	PC7
AIGND	2	52	GND
ACH0	3	53	PC6
ACH8	4	54	GND
ACH1	5	55	PC5
ACH9	6	56	GND
ACH2	7	57	PC4
ACH10	8	58	GND
ACH3	9	59	PC3
ACH11	10	60	GND
ACH4	11	61	PC2
ACH12	12	62	GND
ACH5	13	63	PC1
ACH13	14	64	GND
ACH6	15	65	PC0
ACH14	16	66	GND
ACH7	17	67	PB7
ACH15	18	68	GND
AISENSE	19	69	PB6
DAC0OUT	20	70	GND
DAC1OUT	21	71	PB5
RESERVED	22	72	GND
AOGND	23	73	PB4
DGND	24	74	GND
DIO0	25	75	PB3
DIO4	26	76	GND
DIO1	27	77	PB2
DIO5	28	78	GND
DIO2	29	79	PB1
DIO6	30	80	GND
DIO3	31	81	PB0
DIO7	32	82	GND
DGND	33	83	PA7
+5 V	34	84	GND
+5 V	35	85	PA6
SCANCLK	36	86	GND
EXTSTROBE*	37	87	PA5
PFI0/TRIG1	38	88	GND
PFI1/TRIG2	39	89	PA4
PFI2/CONVERT*	40	90	GND
PFI3/GPCTR1_SOURCE	41	91	PA3
PFI4/GPCTR1_GATE	42	92	GND
GPCTR1_OUT	43	93	PA2
PFI5/UPDATE*	44	94	GND
PFI6/WFTRIG	45	95	PA1
PFI7/STARTSCAN	46	96	GND
PFI8/GPCTR0_SOURCE	47	97	PA0
PFI9/GPCTR0_GATE	48	98	GND
GPCTR0_OUT	49	99	+5 V
FREQ_OUT	50	100	GND

Figure 2. I/O Connector Pin Assignment for the 6025E

Figure 3 shows the pin assignments for the 68-pin extended digital connector. This is the other 68-pin connector available when you use the SH1006868 cable assembly with the 6025E.



GND	34	68	PC7
PC6	33	67	GND
PC5	32	66	GND
GND	31	65	PC4
PC3	30	64	GND
PC2	29	63	GND
GND	28	62	PC1
PC0	27	61	GND
PB7	26	60	GND
GND	25	59	PB6
PB5	24	58	GND
PB4	23	57	GND
GND	22	56	PB3
GND	21	55	PB2
PB1	20	54	GND
PB0	19	53	GND
GND	18	52	PA7
PA6	17	51	GND
PA5	16	50	GND
GND	15	49	PA4
PA3	14	48	GND
PA2	13	47	GND
GND	12	46	PA1
PA0	11	45	GND
+5 V	10	44	GND
N/C	9	43	N/C
N/C	8	42	N/C
N/C	7	41	N/C
N/C	6	40	N/C
N/C	5	39	N/C
N/C	4	38	N/C
N/C	3	37	N/C
N/C	2	36	N/C
N/C	1	35	N/C

Figure 3. 68-Pin Extended Digital Connector Pin Assignments

Caution ***Connections that exceed any of the maximum ratings of input or output signals on the boards can damage the board and the computer. Maximum input ratings for each signal are given in the Protection column of Table 2. National Instruments is NOT liable for any damages resulting from such signal connections.***

Table 1 shows the I/O connector signal descriptions for the 6023E, 6024E, and 6025E.

Table 1. I/O Connector Signal Descriptions

Signal Name	Reference	Direction	Description
AIGND	—	—	Analog Input Ground—These pins are the reference point for single-ended measurements in RSE configuration and the bias current return point for differential measurements. All three ground references—AIGND, AOGND, and DGND—are connected together on your board.
ACH<0..15>	AIGND	Input	Analog Input Channels 0 through 15—Each channel pair, ACH<*i*, *i*+8> (*i* = 0..7), can be configured as either one differential input or two single-ended inputs.
AISENSE	AIGND	Input	Analog Input Sense—This pin serves as the reference node for any of channels ACH <0..15> in NRSE configuration.
DAC0OUT[1]	AOGND	Output	Analog Channel 0 Output—This pin supplies the voltage output of analog output channel 0.
DAC1OUT[1]	AOGND	Output	Analog Channel 1 Output—This pin supplies the voltage output of analog output channel 1.
AOGND	—	—	Analog Output Ground—The analog output voltages are referenced to this node. All three ground references—AIGND, AOGND, and DGND—are connected together on your board.
DGND	—	—	Digital Ground—This pin supplies the reference for the digital signals at the I/O connector as well as the +5 VDC supply. All three ground references—AIGND, AOGND, and DGND—are connected together on your board.
DIO<0..7>	DGND	Input or Output	Digital I/O signals—DIO6 and 7 can control the up/down signal of general-purpose counters 0 and 1, respectively.
PA<0..7>[2]	DGND	Input or Output	Port A bidirectional digital data lines for the 82C55A programmable peripheral interface on the 6025E. PA7 is the MSB. PA0 is the LSB.
PB<0..7>[2]	DGND	Input or Output	Port B bidirectional digital data lines for the 82C55A programmable peripheral interface on the 6025E. PB7 is the MSB. PB0 is the LSB.
PC<0..7>[2]	DGND	Input or Output	Port C bidirectional digital data lines for the 82C55A programmable peripheral interface on the 6025E. PC7 is the MSB. PC0 is the LSB.
+5 V	DGND	Output	+5 VDC Source—These pins are fused for up to 1 A of +5 V supply. The fuse is self-resetting.
SCANCLK	DGND	Output	Scan Clock—This pin pulses once for each A/D conversion in scanning mode when enabled. The low-to-high edge indicates when the input signal can be removed from the input or switched to another signal.

Table 1. I/O Connector Signal Descriptions (Continued)

Signal Name	Reference	Direction	Description
EXTSTROBE*	DGND	Output	External Strobe—This output can be toggled under software control to latch signals or trigger events on external devices.
PFI0/TRIG1	DGND	Input	PFI0/Trigger 1—As an input, this is one of the Programmable Function Inputs (PFIs). PFI signals are explained in the Timing Connections section in the *6023E/6024E/6025E User Manual*.
		Output	As an output, this is the TRIG1 (AI Start Trigger) signal. In posttrigger data acquisition sequences, a low-to-high transition indicates the initiation of the acquisition sequence. In pretrigger applications, a low-to-high transition indicates the initiation of the pretrigger conversions.
PFI1/TRIG2	DGND	Input	PFI1/Trigger 2—As an input, this is one of the PFIs.
		Output	As an output, this is the TRIG2 (AI Stop Trigger) signal. In pretrigger applications, a low-to-high transition indicates the initiation of the posttrigger conversions. TRIG2 is not used in posttrigger applications.
PFI2/CONVERT*	DGND	Input	PFI2/Convert—As an input, this is one of the PFIs.
		Output	As an output, this is the CONVERT* (AI Convert) signal. A high-to-low edge on CONVERT* indicates that an A/D conversion is occurring.
PFI3/GPCTR1_SOURCE	DGND	Input	PFI3/Counter 1 Source—As an input, this is one of the PFIs.
		Output	As an output, this is the GPCTR1_SOURCE signal. This signal reflects the actual source connected to the general-purpose counter 1.
PFI4/GPCTR1_GATE	DGND	Input	PFI4/Counter 1 Gate—As an input, this is one of the PFIs.
		Output	As an output, this is the GPCTR1_GATE signal. This signal reflects the actual gate signal connected to the general-purpose counter 1.
GPCTR1_OUT	DGND	Output	Counter 1 Output—This output is from the general-purpose counter 1 output.
PFI5/UPDATE*	DGND	Input	PFI5/Update—As an input, this is one of the PFIs.
		Output	As an output, this is the UPDATE* (AO Update) signal. A high-to-low edge on UPDATE* indicates that the analog output primary group is being updated for the 6024E or 6025E.

Table 1. I/O Connector Signal Descriptions (Continued)

Signal Name	Reference	Direction	Description
PFI6/WFTRIG	DGND	Input	PFI6/Waveform Trigger—As an input, this is one of the PFIs.
		Output	As an output, this is the WFTRIG (AO Start Trigger) signal. In timed analog output sequences, a low-to-high transition indicates the initiation of the waveform generation.
PFI7/STARTSCAN	DGND	Input	PFI7/Start of Scan—As an input, this is one of the PFIs.
		Output	As an output, this is the STARTSCAN (AI Scan Start) signal. This pin pulses once at the start of each analog input scan in the interval scan. A low-to-high transition indicates the start of the scan.
PFI8/GPCTR0_SOURCE	DGND	Input	PFI8/Counter 0 Source—As an input, this is one of the PFIs.
		Output	As an output, this is the GPCTR0_SOURCE signal. This signal reflects the actual source connected to the general-purpose counter 0.
PFI9/GPCTR0_GATE	DGND	Input	PFI9/Counter 0 Gate—As an input, this is one of the PFIs.
		Output	As an output, this is the GPCTR0_GATE signal. This signal reflects the actual gate signal connected to the general-purpose counter 0.
GPCTR0_OUT	DGND	Output	Counter 0 Output—This output is from the general-purpose counter 0 output.
FREQ_OUT	DGND	Output	Frequency Output—This output is from the frequency generator output.

* Indicates that the signal is active low

[1] Not available on the 6023E

[2] Not available on the 6023E or 6024E

Table 2 shows the I/O signal summary for the 6023E, 6024E, and 6025E.

Table 2. I/O Signal Summary

Signal Name	Signal Type and Direction	Impedance Input/ Output	Protection (Volts) On/Off	Source (mA at V)	Sink (mA at V)	Rise Time (ns)	Bias
ACH<0..15>	AI	100 GΩ in parallel with 100 pF	42/35	—	—	—	±200 pA
AISENSE	AI	100 GΩ in parallel with 100 pF	40/25	—	—	—	±200 pA
AIGND	AO	—	—	—	—	—	—
DAC0OUT (6024E and 6025E only)	AO	0.1 Ω	Short-circuit to ground	5 at 10	5 at -10	10 V/µs	—
DAC1OUT (6024E and 6025E only)	AO	0.1 Ω	Short-circuit to ground	5 at 10	5 at -10	10 V/µs	—
AOGND	AO	—	—	—	—	—	—
DGND	DO	—	—	—	—	—	—
VCC	DO	0.1 Ω	Short-circuit to ground	1A fused	—	—	—
DIO<0..7>	DIO	—	V_{cc} +0.5	13 at (V_{cc} -0.4)	24 at 0.4	1.1	50 kΩ pu
PA<0..7> (6025E only)	DIO	—	V_{cc} +0.5	2.5 at 3.7min	2.5 at 0.4	5	100 kΩ pu
PB<0..7> (6025E only)	DIO	—	V_{cc} +0.5	2.5 at 3.7min	2.5 at 0.4	5	100 kΩ pu
PC<0..7> (6025E only)	DIO	—	V_{cc} +0.5	2.5 at 3.7min	2.5 at 0.4	5	100 kΩ pu
SCANCLK	DO	—	—	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
EXTSTROBE*	DO	—	—	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
PFI0/TRIG1	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
PFI1/TRIG2	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
PFI2/CONVERT*	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
PFI3/GPCTR1_SOURCE	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
PFI4/GPCTR1_GATE	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu

Table 2. I/O Signal Summary (Continued)

Signal Name	Signal Type and Direction	Impedance Input/ Output	Protection (Volts) On/Off	Source (mA at V)	Sink (mA at V)	Rise Time (ns)	Bias
GPCTR1_OUT	DO	—	—	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
PFI5/UPDATE*	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
PFI6/WFTRIG	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
PFI7/STARTSCAN	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
PFI8/GPCTR0_SOURCE	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
PFI9/GPCTR0_GATE	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
GPCTR0_OUT	DO	—	—	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
FREQ_OUT	DO	—	—	3.5 at (V_{cc}-0.4)	5 at 0.4	1.5	50 kΩ pu

AI = Analog Input DIO = Digital Input/Output pu = pullup
AO = Analog Output DO = Digital Output

Note: The tolerance on the 50 kΩ pullup and pulldown resistors is very large. Actual value may range between 17 kΩ and 100 kΩ.

Support

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322153B-01 Dec98